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REPORT SD-TR-89-07

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AD-A206 266

On-Orbit Observations of Single-Event Upset in Harris HM-6508 RAMs: An Update

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16 February 1989

Prepared for

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This report was submitted by The Aerospace Corporation, El Segundo, CA 90245, under Contract No. F04701-85-C-0086-P00019 with the Space Division, P.O. Box 92960, Los Angeles, CA 90009-2960. It was reviewed and approved for The Aerospace Corporation by H. R. Rugge, Director, Space Sciences Laboratory.

Lt Clarence V. Wilcox was the project officer for the Mission-Oriented Investigation and Experimentation (MOIE) Program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

ADA206266

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: Unclassified

1b. RESTRICTIVE MARKINGS:

2a. SECURITY CLASSIFICATION AUTHORITY:

2b. DECLASSIFICATION / DOWNGRADING SCHEDULE:

3. DISTRIBUTION / AVAILABILITY OF REPORT: Approved for public release; distribution unlimited.

4. PERFORMING ORGANIZATION REPORT NUMBER(S): TR-0088(3940-05)-5

5. MONITORING ORGANIZATION REPORT NUMBER(S): SD-TR-89-07

6a. NAME OF PERFORMING ORGANIZATION: The Aerospace Corporation Laboratory Operations

6b. OFFICE SYMBOL (If applicable):

7a. NAME OF MONITORING ORGANIZATION: Space Division Air Force Systems Command

6c. ADDRESS (City, State, and ZIP Code): 2350 E. El Segundo Blvd. El Segundo, CA 90245

7b. ADDRESS (City, State, and ZIP Code): Los Angeles Air Force Base P. O. Box 92960 Los Angeles, CA 90009-2960

8a. NAME OF FUNDING / SPONSORING ORGANIZATION:

8b. OFFICE SYMBOL (If applicable):

9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: F04701-85-C-0086-P00019

8c. ADDRESS (City, State, and ZIP Code):

10. SOURCE OF FUNDING NUMBERS

PROGRAM ELEMENT NO	PROJECT NO	TASK NO	WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification): On-Orbit Observations of Single-Event Upset in Harris HM-6508 RAMs: An Update

12. PERSONAL AUTHOR(S): J. Bernard Blake and R. Mandel

13a. TYPE OF REPORT:

13b. TIME COVERED FROM ______ TO ______

14. DATE OF REPORT (Year, Month, Day): 1989 February 16

15. PAGE COUNT: 8

16. SUPPLEMENTARY NOTATION:

17. COSATI CODES

FIELD	GROUP	SUB-GROUP

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number):
Single event upset (SEU)
Random access memories (RAMs)
Radiation effects in space

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The observed single-event-upset rate of Harris HM-6508 RAMs in a low polar orbit is presented. These data were acquired during a four-year period from 1983 through 1986.

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT: ☒ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS

21. ABSTRACT SECURITY CLASSIFICATION:

22a. NAME OF RESPONSIBLE INDIVIDUAL:

22b. TELEPHONE (Include Area Code):

22c. OFFICE SYMBOL:

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE

UNCLASSIFIED

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Accession For
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Unannounced
Justification
By
Distribution/
Availability Codes
Avail and/or
Dist Special
A-1

I. INTRODUCTION

The single event upset (SEU) phenomenon has continued to be of great interest to designers of spaceflight hardware. Although a great deal of ground testing has been and continues to be carried out, quantitative on-orbit measurements are very limited. Space measurements are a key part of the effort to ensure that the ground-based testing yields accurate predictions of on-orbit upset rates. Blake and Mandel[1] have published data from two years of flight observations from a subsystem consisting of 384 Harris HM-6508 1K RAMs. This report is an update of that study; the results of 2560 days of observation are presented.

[1] J. B. Blake and R. Mandel, Proc. IEEE Trans. Nucl. Sci., 33 (6), 1616 (1986).

II. THE EXPERIMENT

The Harris HM-6508 1K x 1 RAMs are in a satellite subsystem in low, polar orbits. The memory module used in the subsystem containing the RAMs consists of three printed circuit cards with each card containing eight 2K byte memory hybrids for a total of 48K bytes. Thus, each memory hybrid contains 16 HM-6508 RAM chips.

On a regular basis, all but 256 bytes of the 48K bytes are examined for bit errors. Two different techniques are used for detecting bit errors. The first technique, a memory check sum, is capable of automatically detecting all single-bit and some double-bit errors that occurred within a page of memory. A memory page consists of 256 bytes. Memory check-sum tests are performed approximately every 90 minutes. To detect a multiple error or to determine the exact location of the bit error within the page, the entire contents of the memory are dumped and compared to the load file. Memory dumps are normally performed once a month, or immediately after the check sum routine detects an error. Once the location of the error is found, the correct value is reloaded into the memory. After the memory is reloaded, the contents of the memory location in question are verified to determine if the error was a soft error generated by an SEU, a hard error generated by a part failure, or a cosmic-ray-induced latchup.

III. RESULTS

A total of 234 SEUs were observed during 2560 days of observation. Thus, the average upset rate per day is

$$(2.62 \pm 0.17) \times 10^{-7} \text{ upsets/bit day.}$$

The distribution of upsets as a function of time is given in Figure 1.

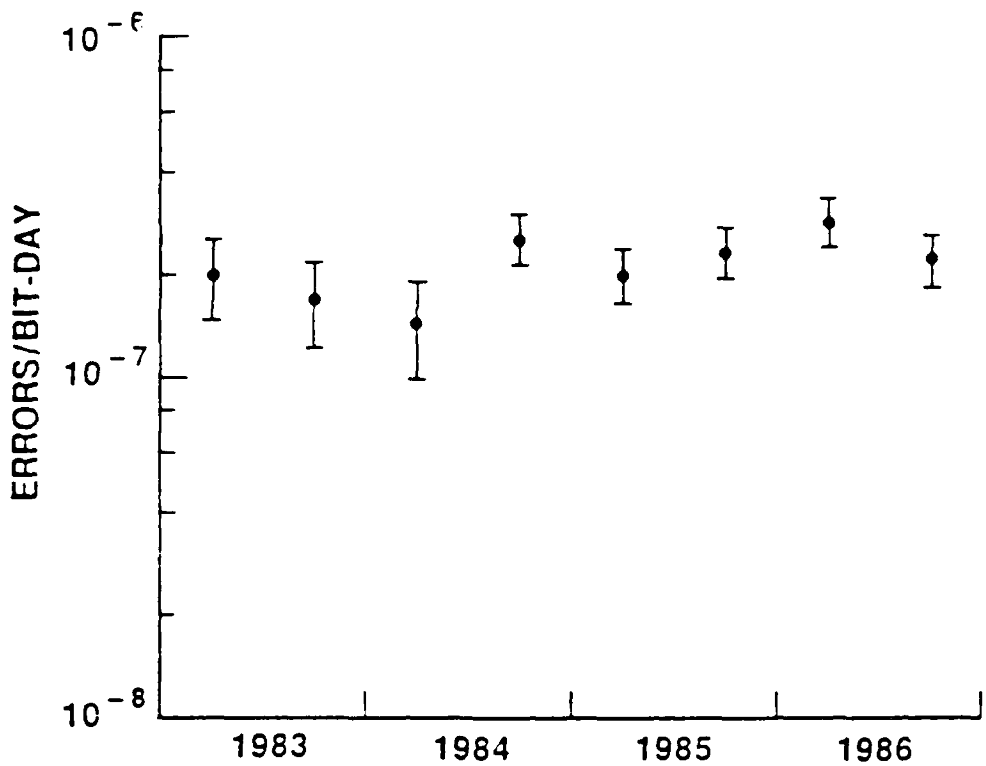

Figure 1. Measured Upset Rate as a Function of Time

The data have been grouped into six-month bins as a compromise between time resolution and counting statistics. Solar cycle modulation can be seen to be modest at best; a horizontal straight line is not a bad fit to the data. A computer code written by Adams* has been used to predict the on-orbit upset rate. The RAM input data are based on accelerator testing of the HM-6508 RAMs; the data were discussed by Blake and Mandel.[2] Some results of the calculation for shielding thicknesses of 1, 2, and 5 gm/cm^2 of aluminum are given in Figure 2.

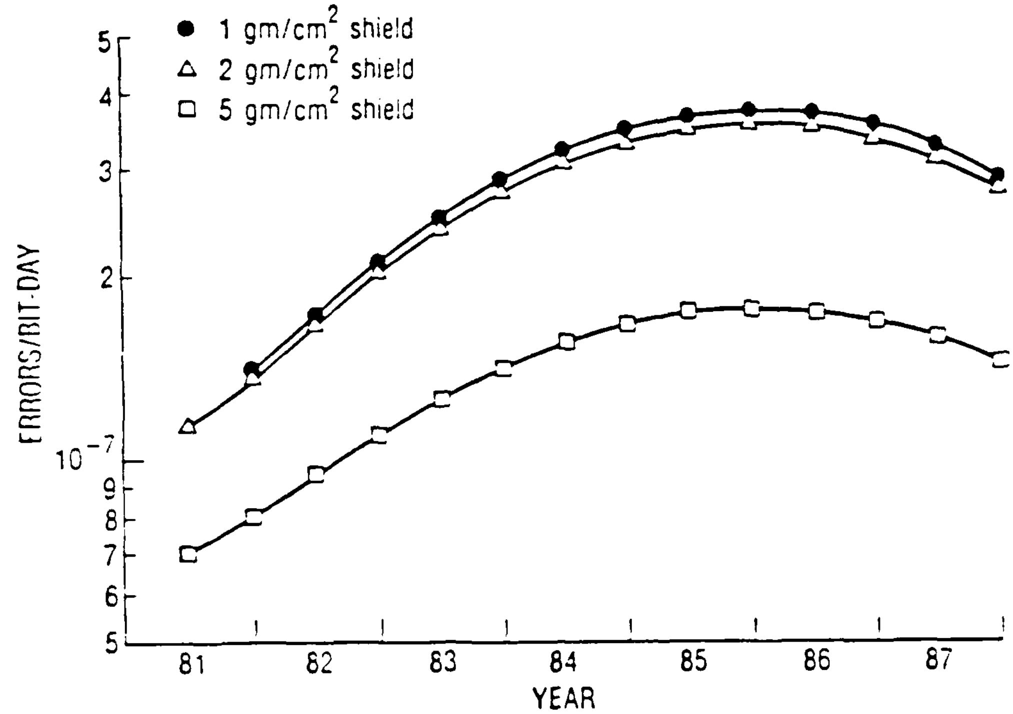

Figure 2. Calculated Upset Rates as a Function of Shield Thickness

It can be seen that the observed SEU rate, given above, is consistent with a shielding thickness of a few gm/cm^2, which is a reasonable value for the

*J. H. Adams, Jr., private communication, 1985.
[2]See Ref. 1.

satellite in question. The predicted solar-cycle modulation may be greater than that observed, although the issue is unclear given the counting statistics.

Multiple events were observed in 14 percent of the upsets. The multiplicity distribution is given in Table 1.

Table 1. SEU Multiplicity Distribution

Number of Events	Multiplicity
202	1
27	2
3	3
1	4
1	All bits on chip

The relative location of the upsets in a multiple event is interesting. In many of the events, the multiple errors were adjacent, including the 4-fold error.[3]

However, in eight cases, the errors were not even on the same board. The obvious question arises: are these multiple SEU events really two independent events that occurred between verifications? As discussed in Blake and Mandel,[1] the probability of such an accidental event is less than once per decade, given the observed upset rate. Perhaps these separated multiple events were due to a single cosmic ray that creates a shower in the satellite vehicle due to a nuclear interaction. An understanding of multiple events will be an important consideration in the effective implementation of error detection and correction techniques in spaceflight hardware.

[3]See Ref. 1.

LABORATORY OPERATIONS

The Aerospace Corporation functions as an "architect-engineer" for national security projects, specializing in advanced military space systems. Providing research support, the corporation's Laboratory Operations conducts experimental and theoretical investigations that focus on the application of scientific and technical advances to such systems. Vital to the success of these investigations is the technical staff's wide-ranging expertise and its ability to stay current with new developments. This expertise is enhanced by a research program aimed at dealing with the many problems associated with rapidly evolving space systems. Contributing their capabilities to the research effort are these individual laboratories:

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